# A temperature compensated linear diode detector

*A simple, yet effective temperature compensated diode detector for large signal applications.*

By Hans Eriksson and Raymond W. Waugh

Schottky diodes are used in many applications as large signal detectors in automatic gain control circuits. A 1997 article [1] describes a self-biased detector having good temperature stability at input power levels higher than 0 dB. It also describes the need for relatively high levels of DC bias to provide temperature compensation at lower input power levels. However, in order to separate the rectified output voltage ($V_o$) from the diode's forward bias voltage ($V_f$), these DC biased detector circuits require a differential amplifier and a reference diode that is carefully matched to the detector diode.

Because of constraints on size and DC power, the self-biased detector is often a preferred approach. Fortunately, a simple detector, with two resistors and a diode in the load, can provide excellent temperature stability and linearity without the use of DC bias.

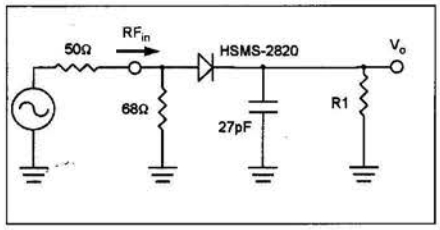


**Figure 1. Simple self-biased detector circuit.**

## The circuit

The simple self-biased detector is shown in Figure 1. If the DC load resistor $R_1$ is set to a relatively low value, such as 4.7 kΩ, the Schottky diode will generate its own bias current at input power levels above 0 dBm. The 68 Ω shunt resistor at the input to the diode provides for a wideband impedance match and a return path for the rectified (output) current.

When input power levels are low, the rectified current is insufficient to self-bias the diode, and the output voltage, $V_o$, varies with temperature, as illustraed in Figure. 2. Not only is temperature stability poor at low levels of input power, but compared to the ideal linear response, output linearity deteriorates as well.

The reason for this variation can be explained as follows. The diode is a termination in the RF circuit (to the left of the 27 pF capacitor in Figure 1). In the DC or output equivalent circuit, the diode can be modeled as a voltage source in series with the junction resistance $R_j$. Output voltage $V_o$ can then be expressed as:

$$V_o = V_{rectified}\frac{R_1}{R_1 + R_j}$$

Where $V_{rectified}$ is the rectified voltage (open circuit $V_o$) and $R_1$ is the DC load resistor shown in Figure 1. It can be seen that $V_o$ will drop when $R_j > R_1$.

In the small signal region, where rectified current is very small (–30 dBm or less), the Schottky diode junction resistance is given by:

$$R_j = \frac{nkT}{q(I_s + I_b)}$$

where $n$ = diode ideality factor
$k$ = Boltzmann's constant
$T$ = temperature in Kelvins
$q$ = the electronic charge
$I_s$ = diode saturation current
$I_b$ = external bias current

Saturation current for n-type Schottky detectors is very small, typically around 1.5 x $10^{-8}$ A. In this analysis, external bias current is zero. When these values are put into equation (2), the resulting value of junction resistance at room temperature is approximately 1.7 MW. Since saturation current is highly temperature-dependent [2], $R_j$ will be even higher at lower temperatures.

As input power is increased from –30 dBm, some circulating (rectified) current exists and the value of $R_j$ goes down. A non-linear analysis can be used to calculate the value of $R_j$ as a function of input power for the self-biased detector, as illustrated in Figure 3.

In most detector applications, $R_1$ is in the range of 1 kΩ to 50 kΩ. As can be seen when values of $R_j$ from Figure 3 are plugged into equation (1), $V_o$ will begin to deviate from the ideal linear response and become temperature-dependent as input power levels drop

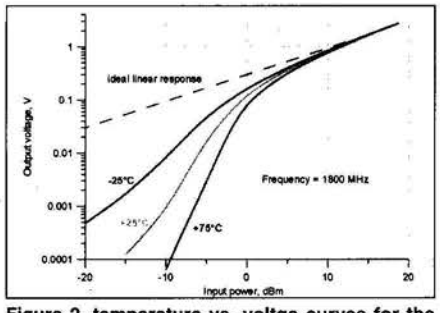


**Figure 2. temperature vs. voltge curves for the detector circuti.**

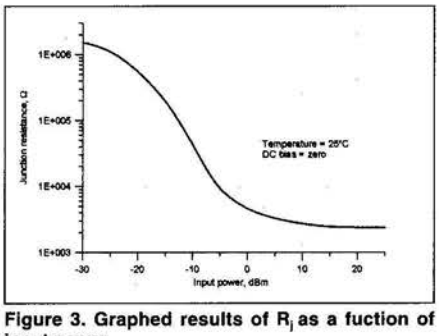


**Figure 3. Graphed results of $R_j$ as a fuction of input power.**

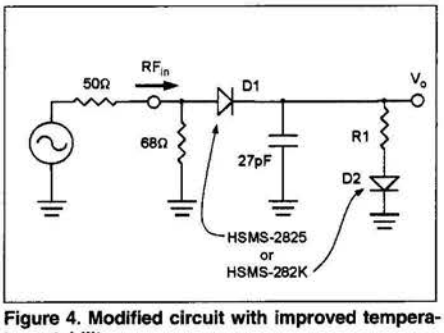


**Figure 4. Modified circuit with improved temperature stability.**

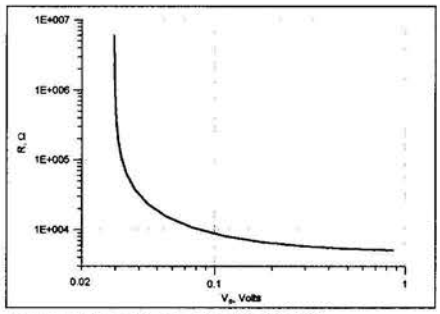


Figure 5. Circuit with $R_1$ set to 4.7 kΩ

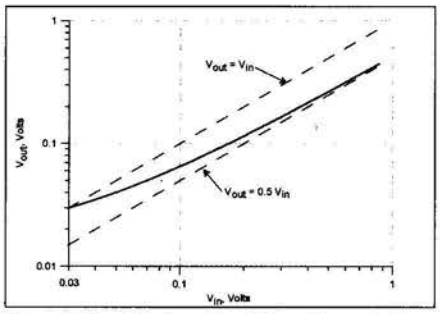


Figure 8. Graphical results of the voltage divider.

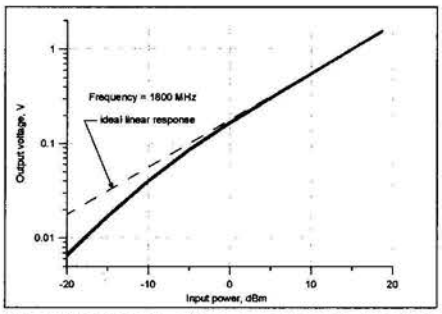


Figure 11. Results of the experimental circuit to verify simulated results.

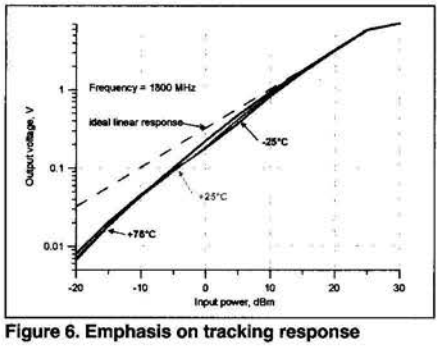


Figure 6. Emphasis on tracking response

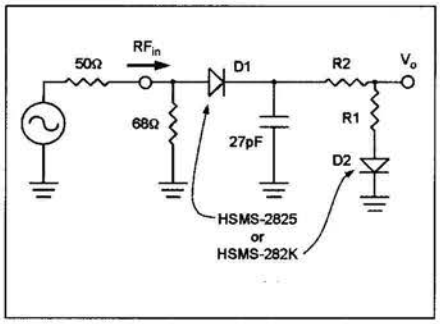


Figure 9. Graphical results of the linearized detector.

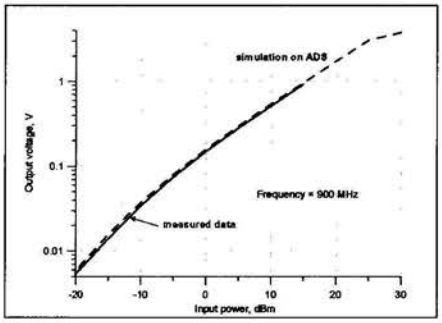


Figure 12. Results of the simulated circuit at 900 MHz.

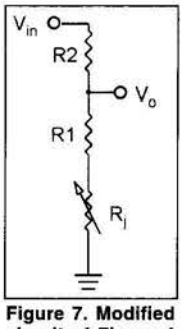


Figure 7. Modified circuit of Figure 4 with components replaced.

below –5 dBm.

## The variable load circuit

An examination of equation (1) leads to the conclusion that a detector circuit with a variable load ($R_1$), one which tracks $R_j$, will result in improved temperature stability. Such a circuit is found in Figure 4. In this detector, a second diode, $D_2$, is added to the DC portion of the circuit. The current produced by rectification in the detector diode, $D_1$, also passes through $D_2$, which acts as a variable load resistor, following the relation given in equation (2). At low values of input power and/or ambient temperature, rectified current will be small, $R_j$ in $D_2$ will be high and $V_o$ will be increased compared to that in the simple detector of Figure 1. When $R_1$ = 4.7 kΩ, the DC load presented to detector diode $D_1$ is shown in Figure 5.

Comparing this transfer curve with that shown in Figure 2 illustrates the improvement in temperature stability, as well as detector linearity, at input power levels below 0 dBm. This circuit is useful at input power levels

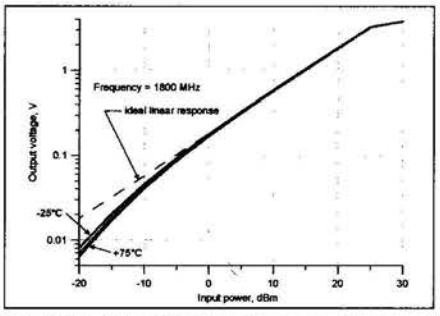


Figure 10. Simulated transfer curve determined by ADS analysis.

under –20 dBm, and offers a large range of input power over which the output is constant with temperature.

While the compensated detector of Figure 4 offers good temperature stability, certain applications might demand even better tracking to the ideal linear response (the dashed line in Figure 6). This might easily be accomplished by replacing the DC load in Figure 4 ($R_1$ and $D_2$) with a variable voltage divider, as shown in Figure 7.

$R_j$ in this circuit is the current-controlled junction resistance of diode $D_2$. At low values of detected signal ($V_{in}$), $R_j$ will be very high and $V_o = V_{in}$. At high input power levels, which raise the value of rectified current and $V_{in}$, $R_j$ will become small compared to $R_1$ and $R_2$. In the event that $R_1 = R_2$, $V_o$ = 0.5 $V_{in}$. The result is that the output voltage shown in Figure 6 for Pin = –20 dBm is unaffected, while the higher output voltage ($P_{in}$ > 10 dBm) is cut in half, improving linearity. The action of the variable voltage divider is shown in Figure 8 for the case in which $R_1 = R_2$ = 4.7 kΩ.

The addition of this variable voltage divider to the circuit results in the linearized detector shown in Figure 9. An ADS analysis of this detector results in the simulated transfer curve shown in Figure 10. Both $R_1$ and $R_2$ were set to 4.7 kΩ. Comparing this performance with that given in Figure 6, one can immediately see the improvement in linearity, as well as some improvement in temperature stability. The simulation predicts near-perfect linearity and almost no variation with temperature for input power levels of –10 dBm or higher.

To verify the accuracy of the simulation, an experimental circuit was built and tested over temperature using a matched pair of representative diodes. The results are given in Figure 11.

The measured data shows slightly inferior linearity and slightly better temperature stability than predicted by the harmonic balance simulation. It is difficult to separate the three curves for –25 °C, +25 °C and +75 °C in Figure 11.

In all other respects, the data obtained in the lab correspond closely to the ADS simulation.

Figure 12 shows the results of the same circuit simulated and tested at 900 MHz. As can be seen, linearity is excellent, as is the correspondence between simulation and experimental data.

Figure 13 illustrates two possible physical circuit layouts. The first uses a derivation of the standard circuit with the polarity of one diode reversed, in the SOT-143 four-lead package. The second uses a derivation of the standard circuit with its grounded center bar serving to provide RF isolation between the detector diode $D_1$ and the compensating diode $D_2$.

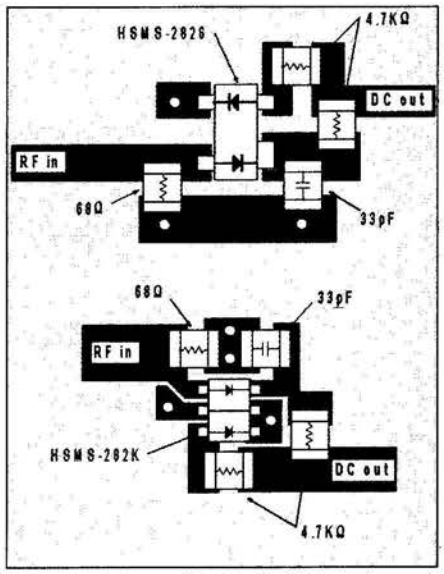


**Figure 13. Two possible physical layouts for such circuits.**

*RF*

## References:


[1] Raymond W. Waugh, "Designing Large-Signal Detectors for Handsets and Base Stations," *Wireless Systems Design*, Vol. 2, No. 7, July 1997, pp 42 - 48.

[2] Raymond W. Waugh and Rolando R. Buted, "The Zero Bias Schottky Diode Detector at Temperature Extremes - Problems and Solutions," Proceedings of the WIRELESS Symposium, 1996, pp 175 - 183


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